Final Report

Analog Time-Division Multiplexer

SD0703

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1 Background:

The purpose of this project is to give Dr. Farden a tool to further his Time-Reversal Signal Processing (TRSP) research. The Analog Time-Division Multiplexer's (ATDM) role is to first organize up to four audio signals onto a composite broadband signal. Then this composite signal may be sampled by Dr. Farden's GNU radio and time reversed. At this point, the ATDM can accept the updated broadband composite signal and reconstruct each time-reversed audio signal.

For futher reading, Wikipedia's page "Time Reversal Signal Processing" provides a good overview of the technique.

2 Requirements:

1. Receive 4 low-level real 20 KHz bandwidth audio signals.
2. Organize input signals as an analog time-division multiplexed signal (a single composite signal).
3. Transmit and re-organize the single composite broadband signal to the original 4 audio signals.
4. The demultiplexed signals in a test configuration should be accurate to the originals within a LSB of a 12 bit A/D converter: i.e.,

   $$| \text{ max error } | \leq \frac{\text{Peak-to-peak voltage of the input}}{2^{12}}$$

   for possible future interface with gnuradio.
   http://www.gnu.org/software/gnuradio/
5. Sampling of all 4 channels must occur simultaneously.

3 Detailed Descriptions:

3.1 403 Design Considerations.

3.1.1 Signal Filtering

(Author: Landon. Primary Contributor: Landon.) The first design consideration was what type of low pass filter to use for band-limiting the input and output signals (see figure 1). Band-limiting the input/output signal is an important step in our design. If we don't ensure all 32 channels are limited to a maximum bandwidth aliasing may result when the signals are sampled. The filters considered for this application were Butterworth, Chebyshev I, Chebyshev II, and Elliptical. We were most concerned with how each filter behaves in the pass and stop bands more than how quickly they transition from one to

another. For this reason Chebyshev II and Elliptical filters take themselves out of consideration. Both of these filters have ripple behavior in the stop bands. This is unacceptable because this stop-band ripple behavior will result in aliasing. The choice is between Butterworth and Chebyshev I implementation. A Butterworth filter has the distinction of being maximally flat in the pass band when a Chebyshev I filter has ripple behavior in the pass band. A Chebyshev I filter has the distinction of having a much tighter transition region between the pass and stop-bands than a Butterworth filter of the same order. The Butterworth filter was decided on because the Chebyshev I distortion in the pass band caused by the ripple behavior is not desirable due to Dr. Farden's signal accuracy requirement. Also, the transition region of a Butterworth filter can be tightened up to an acceptable range by implementing higher order filters. While researching the implementation of active 2nd order Butterworth filters we came across 4th order unity-gain Butterworth filters-on-a-chip from Linear Technology. These were attractive chips because of the following reasons.

1. A 4th order filter was likely of a high enough order for an adequate transition region between pass and stop bands.

2. The physical size of the circuit would be smaller than a filter of the same order built of op-amps and feedback networks.

3. Achieving good filter characteristics for all 32 channels would be easier with this chip than it would be with op-amps and external feedback networks for every stage on every single channel

Two samples of LTC 1563-2 were requested and received from Linear Technology. Physically the chips are surface mount and very small, approximately 0.15 x 0.19 millimeters. This made testing the chips more difficult than bread-boarding the tuning resistors into the chip. To test the chip we had two options. The first was to order Schmart Boards. Schmart Boards are printed circuit boards (PCB) that effectively fan-out the chip pins to a point where headers may be soldered to the pins. The other option was to design a layout on Ultiboard and fabricate a PCB in-house. The second option was carried out. I decided on this option because I wanted to test the chips in an environment that is as close to their final environment as possible. Without fabricating a PCB regular through-hole resistors would have to be bread-boarded and placed in the circuit. I spent many hours in Ultiboard to come up with an acceptable layout. The first step was learning how to create a new footprint in Ultiboard specifically for the chip as a matching footprint could not be found. The next step was deciding on how to best place components. The last step was reworking the layout numerous times as fabricating the small PCB repeatedly failed.

3.1.2 Sample & Hold

(Author: Landon. Primary Contributor: Landon.) The sample and hold chips are LF398. These chips were first considered because they are well established chips and were recommended by Dr. Farden. Another advantage of investigating

these chips was they were already in house. The datasheets suggested they were capable for our project or at least capable enough to begin working with them. A number of considerations were involved with the sample & hold implementation. The first topic covered will be the hold capacitor. Deciding on the capacitor value we are currently using was relatively easy. To begin I selected the smallest capacitor value listed in the data sheet range. The trade-off with capacitor selection was acquisition time versus capacitor droop time. A smaller capacitor would have a quicker acquisition time than a larger capacitor. However this comes at the cost of not being able to accurately hold its value as long. The way the datasheets read for our application capacitor droop would not be much of an issue at any value. The analog value is being held for a relatively short time before the circuit re-enters sample mode. So the task was to select a capacitor that could acquire a signal quickly enough. But as the project progressed a quick acquisition time became less critical. This is a result of the two bank sample and hold system implemented which will be covered next. Currently the capacitor value is 0.001 F. Another issue with the sample and hold circuitry is timing. Some sort of waveform needs to be generated to control the signal acquisition. Dr. Farden's design requirements dictate that all 32 channels must be sampled simultaneously. This is for a good reason. The system is meant to be used in time-reversal signal processing applications. Because of that it is important that even though the signals are placed successively on the composite line the successive values must be taken simultaneously. This made timing more complicated than it would have been if each channel could have been sampled just before it is placed on the line. The original plan was to use one sample and hold chip per channel. This introduces a problem. The multiplexer cannot be allowed to place signals on the line when the chips are all in sample mode. This means that once per sampling period there would be considerable time when information cannot be placed on the line. Dr. Farden proposed a way to avoid this. He suggested implementing a "two - bank" sample and hold system. In this system the first sample and hold chip seen by all 32 channels makes up the first "bank". Only channels 17 - 32 have the second bank. This is the 2nd sample and hold chip cascaded behind the 1st. Refer to figure 3 below for a clear visual. The advantage of this is there will be no dead spot on the line. I will try to make this clear by giving a step by step description of one sampling period.

1. All 32 signals are simultaneously sampled by the sample and hold chip in bank 1.
2. Soon after bank 1 goes into hold mode the multiplexer begins placing signal values on the line starting with channel 1.
3. Before the multiplexer reaches channel 17 (1/2 of the way through the channels) bank 2 has sampled and held the analog value stored on bank 1.
4. While the multiplexer is placing the signal values from channels 17 - 32 on the composite line bank 1 is free to sample all 32 channels once again.

5. This makes up one cycle and it is through this setup that all 32 channels are simultaneously sampled but information can be placed on the line uninterrupted.

The waveforms generated for the sample and hold circuitry are simple. They are two 25% (this was changed in 405) duty cycle square waves, one for each bank and the second is delayed from the first by half the period. Refer to figure 4 below for a clear visual of the waveforms generated.

There are a few notable reasons for using these specific waveforms.

1. Room for error. A close look at figure 4 suggests that signals from channel 1 and channel 17 are not being placed on the composite line instantaneously after each bank enters hold mode. A 25% duty cycle allows the value on the sample and hold chip to settle before they are placed on the line. Ideally a 50% duty cycle could be used but it is obvious this would allow no settling time before the first channels on each bank are sampled as well as it would introduce the possibility of circuitry reentering sample mode before the last channel on each bank is placed on the line.

2. Ease of waveform generation. As mentioned above 50% duty cycle waveforms are not a good idea. The next easiest waveform to generate is a 25% duty cycle. This has been accomplished using a binary counter chip as a clock divider and a few gates. More specifically the gates are two input AND gates and an inverter. Figure 5 clearly illustrates that a 25% duty cycle square wave at the frequency of one-fourth the clock frequency can be generated at the output of an AND gate whose inputs are CLK \ 2 and CLK \ 4. The resulting waveform is shown labeled Bank 1 in figure 4. The waveform for Bank 2 in figure 4 is generated by running CLK \ 4 through an inverter before applying it to another AND gate. The inverted CLK \ 4 is the waveform labeled (CLK \ 4) ' in figure 5.

3.1.3 Band pass filter design

(Author: Matthew, Primary Contributor: Matthew) A crucial property of our working analog time division multiplexer is to synchronize our multiplexer and de-multiplexer. Synchronization for our purposes consists of the clocks controlling the multiplexer and de-multiplexer to be operating at the same frequencies. To make this idea realizable a global clock outputting square pulses will be used to control the multiplexer and will also be fed into a band pass filter. The center frequency f_C of the band pass filter is planned to be set at $3f_C$ to pick off the 3rd harmonic of the global clock. The reason why we can't simply just place our clock through to the de-multiplexer is because the multiplexer will use a lot of bandwidth so we will need to be sure that the clock will be separated from all other frequencies. The resulting output will be a sinusoid B(t) at $f = 3f_C$ to be input into the de-multiplexer stage along with the composite output of the multiplexer $x_c(t)$. The sinusoid and composite signal will then be sent into the de-multiplexer stage as the sum $x_C(t) + B(t)$. The sum of both signals

will be sent into a low pass filter and also a band pass filter. The band pass filter will be used to filter away $x_C(t) from B(t)$ and the low pass filter will be used to filter away B(t) and allow xc(t) to be fed into the de-multiplexer. After B(t) is filtered off from $x_C(t)$ it can be used to generate sgn(B(t)) through a comparator or equivalent circuit. This will then output a square wave at $3f_C$ to be used as the global clock at the de-multiplexer. Both passive and active filters were initially considered for implementing a band pass filter. While active filters may be simpler to mass produce(IC form) with the same pass band, a carefully devised passive filter may offer a degree of higher precision for the center frequency. An active filter also utilizes more components than a passive filter which can cause more error and offers a greater probability of a component failing. These were the initial reason a passive filter was selected. For the first attempt of the filter design, the center frequency and the capacitor were fixed using the formula $f_O = \frac{1}{2\pi\sqrt{LC}}$, where $f_O = 24$MHz and C = 10pF . The result led to a discrete value of the inductor which was 4.7μH. Although the calculated value for the inductor wasn't common a good approximation was implemented using series/parallel relationships. A network analyzer was used to observe the frequency response for this filter. The center frequency O was off the mark a little bit and when the filter was tested we still picked up an unwanted harmonic (8MHz frequency component). Since the initial filter did not work well enough another approach was taken. The "Q" (Quality) factor is a measure of the sharpness of the roll off from the center frequency. Having a high (sharp) quality factor will allow for a more prominent attenuation of unwanted frequencies relative to the previous result. "Q" is defined as $\frac{1}{R}\sqrt{\frac{L}{C}}$ in a series passive band pass circuit. Looking at the previous equation we can see how simply "Q" can be controlled by manipulating the components. Another concept brought into the second attempt of filter design was the idea of using a ferrite core inductor and wrapping it with copper to get an inductance that can be very close to the computed (theoretical) values. Using this, the desired center frequency was exactly at 24MHz, but still we had the 8MHz frequency component present. In order to obtain a higher "Q" a larger inductance and smaller capacitance were selected as the above equation depicts. With our higher "Q" circuit we were able to obtain a much better attenuation of the fundamental harmonic, but it still was present. The current values for our inductor and capacitor are respectively 17.6μH and 2.5pF. The network analyzer displayed a -37.6dB attenuation at 8MHz, however when we connected it to the 8MHz crystal we were still receiving a prominent harmonic at 8MHz. Adjusting the ratio of L to C is working, because now the 24MHz harmonic has a larger magnitude than the 8MHz harmonic. The next step is get a 1pF capacitor or something very close to that value.

3.1.4 Multiplexer Implementation

(Author: Landon. Primary Contributor: Landon.) The current multiplexer being used is from Analog Devices part number ADG732. It is a 32 channel parallel controlled chip. The waveforms controlling this chip once again come from the 4-bit counter used to generate the sample and hold waveforms. The prototype board that I've built is currently a four channel implementation. Because of this only the two least significant bits of the counter are being used to control the multiplexer.

This concludes the design considerations from 403.

3.2 405 Design Considerations

3.2.1 Scaling 403 work to 32 channels

(Author: Landon. Primary Contributor: Landon.)

The first task of the semester I took on was looking at what was done in 403 and then thinking about how to apply that to what we need in 405. The end product of 403 was a PCB that contained the sample\hold and multiplexer waveform generation as well as the sample\hold circuitry.

When 405 started I looked at whether or not this circuitry was still usable in the context of the increased clock frequency needed for 32 channels. The data sheets for the sample\hold chips told me it wasn't.

This is because the 403 waveform generation had a 25% duty cycle which means the chip had $\frac{1}{4}250kHz^{-1} = 1\mu s$ to track the input signal. Scaling the clock frequency to 8 times the old clock frequency to allow for 32 channels would press the acquisition time to further than what the sample\hold chips could handle according to the datasheets.

As a result the first task I worked on was increasing the duty cycle of the sample & hold logic. I began by looking at the waveforms I had off the binary counters I was using from 403 and tried to figure out a logic that would increase the 25% duty cycle.

The logic used can be seen in figure 1.

This logic ended up working out but caused some problems first. After building the circuit the output was very glitchy. What I mean by that is when the output should have been low (high), there were times when the output would suddenly spike. After simulating the circuit I saw the same behaviour. I am familiar with what causes logic glitches, what a hazard is, and how to fix it so I first went looking for the error. Through Karnaugh Maps I discovered the logic implementation used should theoretically be glitch free. After more work I found out the way I had the binary counters cascaded was wrong and this caused the "glitches" in the logic.

When this issue was cleared up the resulting output is a 37.5% duty cycle square wave which allowed an adequate acquisition time according to the datasheets.

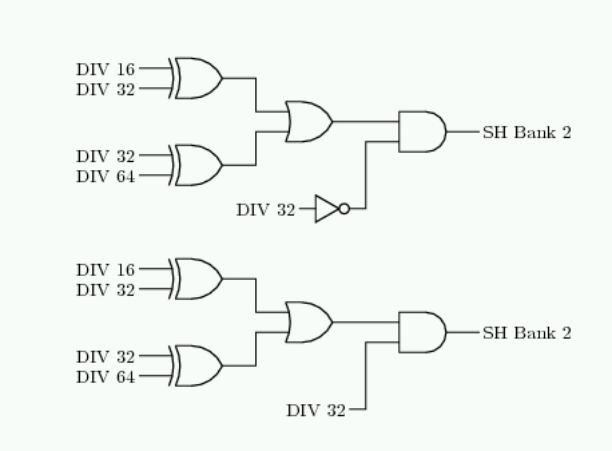

Figure 1: Multiplexer sample & hold waveform generation.

For a four channel multiplexer a 250kHz clock is seen by the multiplexer chip. However, a 1MHz crystal is used and that is divided down by four to generate the clock. It was done this way to help Matt out with his bandpass filter design. Dr. Farden pointed out it would be easier to build a filter for a 1MHz crystal than a 250kHz crystal. The reason for this is even though in theory a square wave should only have odd harmonics of the fundamental frequency, crystals do not yeild ideal square waves. This means there are even harmonics of the fundamental as well. So a bandpass filter for a 250kHz crystal must have a much tighter bandwidth than a bandpass filter for a 1MHz crystal making it harder to build.

It is because of this implementation that the inverters are placed in between the outputs of the binary counter and the multiplexer. In a circuit with no propogation delay only the inverter between the output serving as the clock to the multiplexer and the multiplexer itself is required. This inverter is required because the multiplexer updates on falling edges of the clock and the inverter serves to make sure the falling edge comes away from edges on the channel control bits.

Originally the control bits did not have the two inverters between the counter and the multiplexer. This caused problems due to propogation delay. What happened was the clock now had an added delay through that inverter but the control bits didn't. The result was instead of the channel updating immediately before the control bits changed, with the delay the channel updated immediately after the control bits changed. This meant the state of the multiplexer was off by one with respect to the state of the rest of the circuit. The solution was to invert the control bits twice to add enough of a delay to where everything was in synchronization.

3.2.2 Multiplexer data aquisition PCB layout

(Author: Landon. Primary Contributor: Landon.)

The next task was beginning layout on the low-pass filter and sample & hold boards. There isn't much to cover here, the topology for each channel was known from 403 so it was a matter of ironing out some issues in PADS and fitting everything on one board.

3.2.3 Multiplexer waveform generation PCB layout

(Author: Landon. Primary Contributor: Landon.)

An effort was made to keep the layout tight and simple. The board currently being used was a second revision, the improvements were adding the bit-comparison circuitry, making the board capable of 4 or 8 channels configurable by jumpers, and adding more sample\hold output sockets.

3.2.4 Demultiplexer circuits

(Author: Landon. Primary Contributor: Landon)

The demultiplexer design wasn't something I considered too heavily in 403. When it came crunch time to finalize the design quite a few ideas were discussed between Dr. Farden any myself. The major obstacle to get over involved the implied requirement that all channels must be released simultaneously as they were sampled simultaneously. Dr. Farden and I devised a few ways to do this each with some flaw. I finally came up with what we have now.

The basic premise is this; per channel, there are two sample\hold chips in parallel. Each output goes into a 2 channel multiplexer whose output feeds into the 20kHz reconstruction filters.

Each sample\hold chip has a unique logic waveform. This means for a four channel device, there are eight unique waveforms and sixteen for the eight channel configuration. For the four or eight channel setup these waveforms are generated by one or two decade counters configurable through jumpers.

The result of all of this is that one time through all channels, one sample\hold chip of the pair is acquiring and holding the voltage level on their corresponding frame. Through this entire period, the other sample\hold chip is holding the previously acquired voltage level and the analog switch is passing that level to the reconstruction filter. After all channels have been acquired the analog switches on all channels simultaneously toggle to pass the previously acquired value to the reconstruction filters. Now the opposite sample\hold chip is free to acquire the new voltage value on it's frame.

The decade counters datasheets describe how to limit how high they count if you don't want to count to ten. This just involves wiring the first output you *don't* want to the reset pin. Setting up the circuit in this manner caused some problems however. Due to the same reasons the bit comparison circuit was added a logic had to be set up to reset the counters not based on the previous state of the decade counters but based on the state of the binary counters. This

circuit ensures that the decade and binary counters stay in synchronization. If this circuit wasn't used it was very likely that the sample\hold circuits would acquire a level that is not on its frame.

3.2.5 Demultiplexer layout

(Author: Landon. Primary Contributor: Landon)

With the circuits designed on paper the next step I took was breadboarding a prototype circuit. After this was complete it looked as if everything was working reasonably well so I began transferring that circuit to a layout.

The first board I completed was the signal reconstruction board. This board has 18 channels on it. I did it this way because the analog switches have three 2-channel switches per chip. The intent is two of these boards can be ordered and only 16 channels populated each.

3.2.6 Sum Amp, Pulse Shaping, BPF

(Author: Matthew. Primary Contributor: Matthew)

Shown below are the summing amplifier (Figure 2), the pulse-shaping circuit (Figure 2), and the passive bandpass filter (Figure 2). The bandpass filter shown, attenuates the most outside of the passband (24MHz). There were several other topologies implemented but did not attenuate like the one shown. The inductor for this filter was actually a T37-2 toroid from the website http://toroids.info/T37-2.php with a specified number of turns to achieve this discrete inductance. Even with significant attenuation outside of the passband, the fundamental(8MHz) was still present and only 2.5dB below the $3f_O$(24MHz). Remember that we want the bandpass filter to completely wipe out the fundamental, so that the fundamental does not get summed with the composite signal. Manipulation of the attenuation for the series bandpass filter is done by altering the "Q" factor which is defined as $\mathrm{Q} = \frac{1}{R}\sqrt{\frac{L}{C}}$. Early in Senior Design III another series bandpass filter was theoretically tested, only this time with a frequency of 8MHz. The inductor was selected to be (396μH) with a capacitor (1pF), while R was set equal to 1 to get a Q of roughly 20,000. However this was never put to realization because at the time we were unsure of the fundamental frequency we were going to use. With the help of Dr.Glower the summing amplifier was created to use as the junction where the composite signal and the nth harmonic from the global clock will meet. The summing amplifier did what it was supposed to do, but the major drawback here was the attenuation we were seeing in the output. We input a 250 kHz signal with a Vpp of 1 and an 8MHz signal with a Vpp of 4. The output we were seeing was at about 180mVpp which isn't good. The feedback resistor was doubled (200KΩ) to bump up the output signal to 300mVpp. We could not get the output signal to increase anymore, so a new op-amp or a different feedback scheme may be some ideas for decreasing the attenuation. The pulse-shaping circuit shaping circuit was an idea that Dr.Farden came up with. In order to figure out what values of components we needed we came up with the following scheme. We pretended we were

working with a 2MHz clock since each channel on our multiplexer is sampled for 0.5μs. We chose a clock since it has high frequency content (the goal of the pulse shaping circuit is to limit the bandwidth of our signal). Another goal of ours was that the capacitor be charged at T/2. Landon came up with the idea to now design the components as if we were dealing with a 4MHz clock. Now utilizing this with the RC time constant phenomena we know that at 5*RC, the cap will be fully charged. Setting 5*RC = .125μs, R turned out to be 450 Ω and C was 55pF. After implementing the circuit on breadboard we found the optimal values to have R being equal to 150 Ω and the capacitor equal to 10pF.

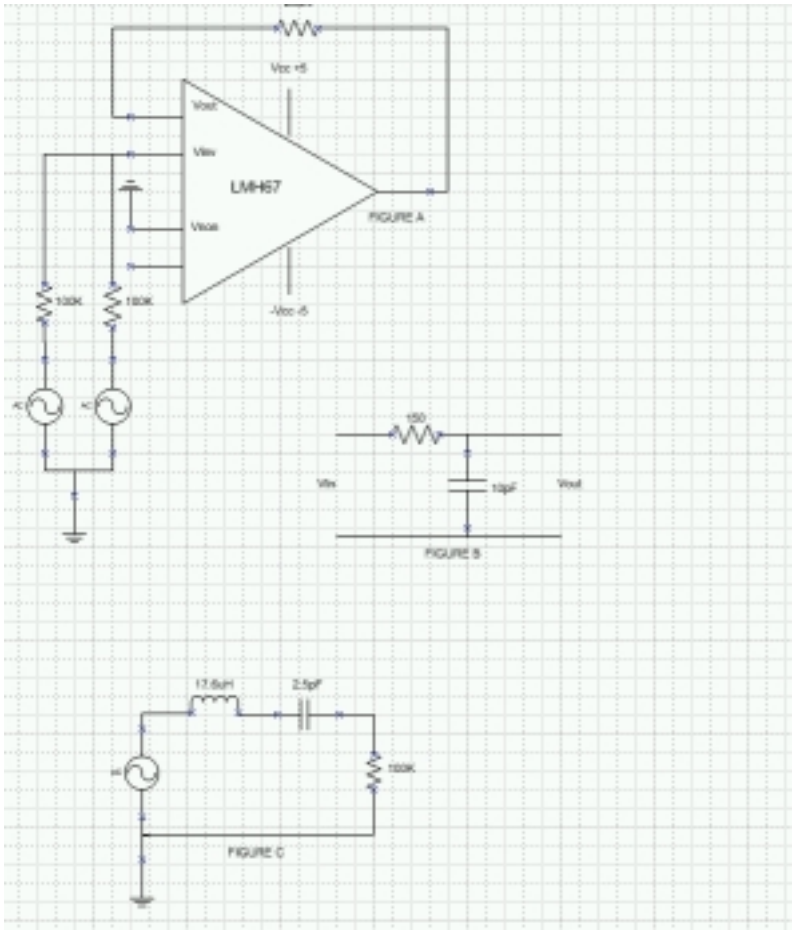

Figure 2: Summing amp, Pulse shaping circuit, BPF

4 Cost:

Part Number	Description	Quantity	Amount
MM74HC86MXCT	2IP EXCL OR GATE	2	$0.86
296-8245-5	4 BIT BINARY COUNTER	6	$0.55
296-9212-5	HEX INVERTER	5	$0.56
296-1093-1	2IP POS-OR GATE	2	$0.40
568-1371-5	AND GATE QUAD 2IP	2	$1.88
296-9849-1	POSITIVE D-TYPE F-F	5	$1.95
MM74HC04	HEX INVERTER	5	$2.10
MM74HC86MXCT	2IP QUAD EXCL OR GATE	5	$2.00
296-1093-1	2IP POS-OR GATE	5	$2.00
568-3072-5	4IP NOR GATE	5	$2.75
296-3576-1	3IP NOR GATE	5	$2.25
478-3353-1	CAP CERM .10μF 50V 20% 1206SMD	500	$49.50
RHM127KFCT	RES 127kΩ $\frac{1}{4}$W 1% 1206SMD	400	$10.92
LTC1563-2CGN	IC FILTER LOPASS 4TH ORD	64	$194.88
LF398S8	IC AMP PREC SAMPLE & HOLD	112	$34.30
18142-2480 Senior Design	PCB MUX2.1-1	1	$52.58
18142-2480 Senior Design	PCB MUX2.1-1	1	$52.58
18142-2480 Senior Design	PCB Clock Board	1	$52.58
568-1371-5	2IP QUAD AND GATE	3	$2.82
MM74HC04M	HEX INVERTER	7	$2.94
497-1131-1	IC MUX\DMUX TRPL 2CH ANLG	15	$7.80
568-2846-5	JOHNSON DECADE COUNTER	10	$7.80
18142-2480 Senior Design	PCB DeMux_Filter	1	$56.98
	Budget Spent	$ -661.07	

5 Block Diagrams:

See figure 3 for the projects block diagram.

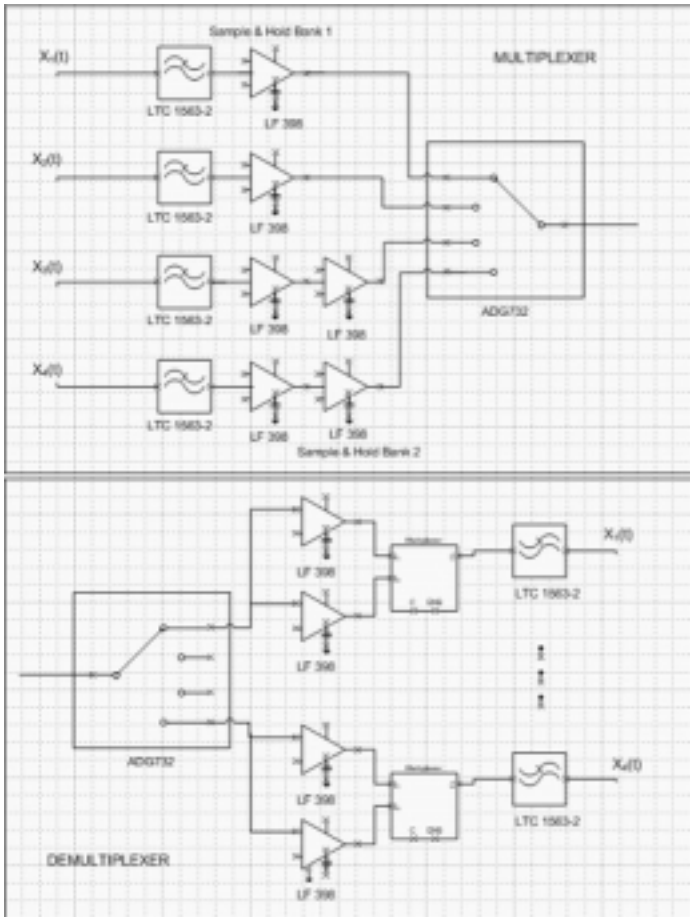

Figure 3: Block diagram.

6 Schematics:

See the appendix for all schematics.

7 Technician's Troubleshooting Section:

1. The first step the user should take is to recheck the User's Manual to ensure that the ATDM has been properly assembled.

If all connections look like they have been made correctly based on the User's Manual it may be useful to probe at least one power pin of each type as well as the digital waveform pins to ensure the connections have been made well. If this all checks out ...

2. Apply an input to the nonfunctioning channel and probe that channel's signals through the device.

   - The lowpass filters should not be a problem assuming the power supplies are present (and at no point have been no greater than ± 11V), there are no shorts between pins, and the chip is still healthy.

     Since the filters require no inputs besides the applied signal (which must fall in the range of $(V^- - 0.3V) \leq V_{PIN} \leq (V^+ + 0.3V)$) and power supplies, nonfunctionality in another part of the circuit should not keep them from working.

     Therefore, if the filter is giving no output for an applied audio signal, check for power, shorts, or consider replacing the chip.

   - If the filters are functioning, check the sample and hold chip. After confirming the power supplies are ok, check the logic pin (8) on the chip.

     If the logic pin 8 is receiving a changing signal and there is still no output it is likely that there is a short somewhere or the chip has been damaged and needs to be replaced.

     If the logic is constantly 0V either the wire is not connected to the board correctly, at all, or there is a problem with the waveform generation logic (see "Digital Issues" below).

   - The next place to check is the multiplexer. Probe channels 1 through 4, as this is a 4 channel device these are the only options.

     If there is no output on one of these channels and assuming the power supply is ok then it is likely either the logic controlling the multiplexer has a problem (see "Digital Issues" below) or at one point there was an overvoltage and the chip may be damaged. If the digital inputs to the chip are present and there is no output the chip has likely been damaged and it will have to be replaced.

   - We have now made it through the multiplexer. To troubleshoot the demultiplexer follow the same procedure above.

3. Digital Issues

   If you encountered a digital logic signal that is a constant 0V while probing the sample & hold circuit and multiplexer the waveform generation boards will have to be probed.

   Begin how you prefer, at the clock input for each board or the nonfunctional output. As this is a two layer board all traces between pins can be seen without consulting a schematic. Note that not all *output* pins on

all chips are used, some may be static. If you find an *output* pin that is static it may just be one of those pins. Continue probing the rest of the *output* pins on the chip. If *all output* pins on that chip are static there is something wrong with that chip.

First check the power supplies. If those are ok make sure the jumpers throughout the circuit are present and connected to either "4 CH" or "8 CH". Of course, all jumpers should be on either 4 or 8 and not a mix between the two.

If a digital logic output is constant then a chip *has to* be the cause. Probing through the board should flush it out and allow you to replace it.

4. Now assuming the digital logic is ok, the analog chips are properly powered and not damaged, and all analog signal connections are ok, make sure:
   (a) you are using the oscilloscope correctly to eliminate the possibility that you have a signal and just are not set up to see it.
   (b) if using speakers at the output, the speakers are set up correctly and not damaged.

8 Comments:

To begin, the ATDM works very well and we think it is a good product for a first attempt. Having said that there are a few things that could use some tweaking. This section will highlight those issues.

8.1 Project Issues

There is only one major project issue that we have run into. This involves the sample & hold chips on the demultiplexer boards. They are adding ≈300mV of dc offset to the applied signals.

As of right now we haven't found the reason for the offset, but since it appears uniformly across all sample & hold circuits on the demultiplexer it must be something in the board layout or possibly the analog switch is pulling up the output for some reason.

This won't affect the audio integrity signal (our ears won't detect it), and since it occurs *after* the GNU radio would finish with the signal it really shouldn't be a major problem. But if the culprit could be identified, future board revisions could compensate for the problem.

8.2 Future Work

One major task that wasn't a part of our requirement but I wanted to accomplish and didn't was to get rid of the clock to the demultiplexer.

What I mean by that is right now the clock signal from the multiplexer is wired into the demultiplexer board. The goal was to:

1. Bandpass filter off the fundamental harmonic of our 8MHz clock,...
2. ...sum the composite output of the multiplexer with the 8MHz sinusoid and,...
3. ...on the demuliplexer side, low-pass filter off the broadband composite message as well as bandpass filter off the 8MHz sinusoid. With that sinusoid, (if necessary) use a comparitor plus a dc offset to generate a demultiplexer clock signal.
4. Finally, employ some circuitry to synchronize the multiplexer and demultiplexer frames.

See Figure 4 for a block diagram of what we would have liked to include.

This part of the project *started* with Matt's bandpass filter which was never finished. As a result work on the rest of the circuitry died.

Having the sinusoid as part of the composite would be helpful for work on the GNU radio. Specifically, it would provide the GNU radio a reference to know what frequency the multiplexer is working on among other uses.

Dr. Farden has a very good understanding (much better than I) of this future work and would be able to guide any further efforts.

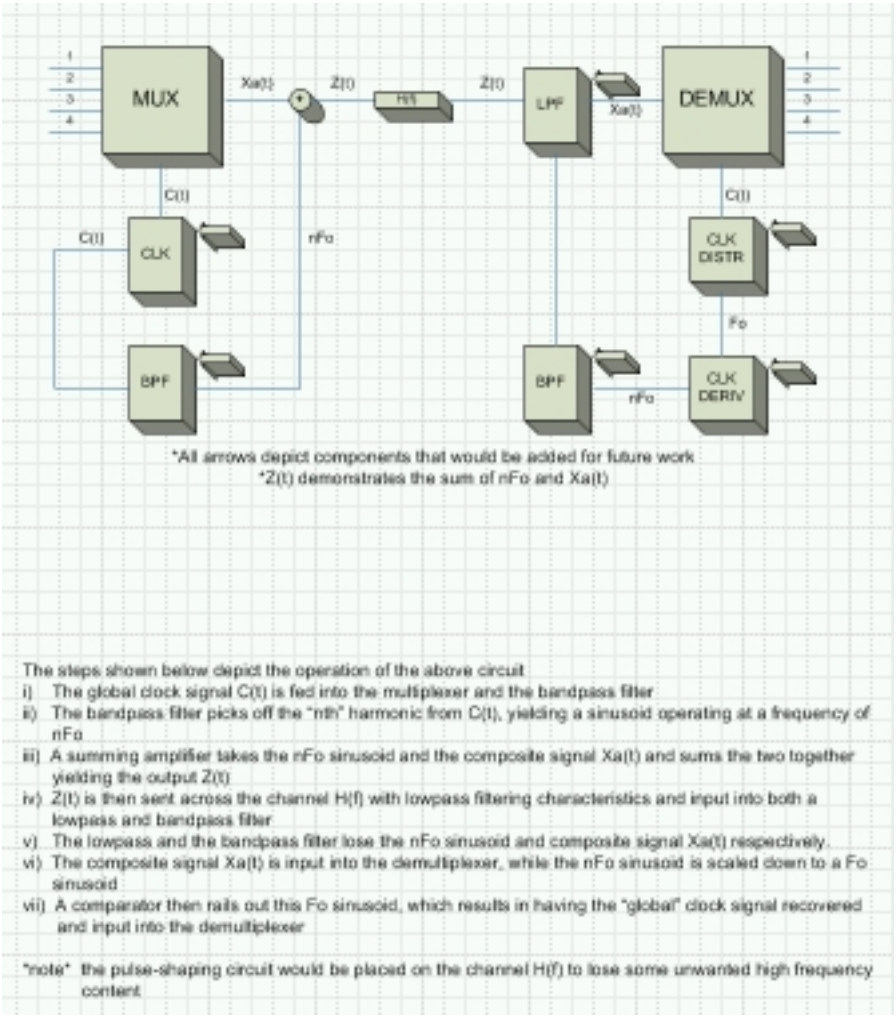

Figure 4: Circuits to be added.

9 Pictures:

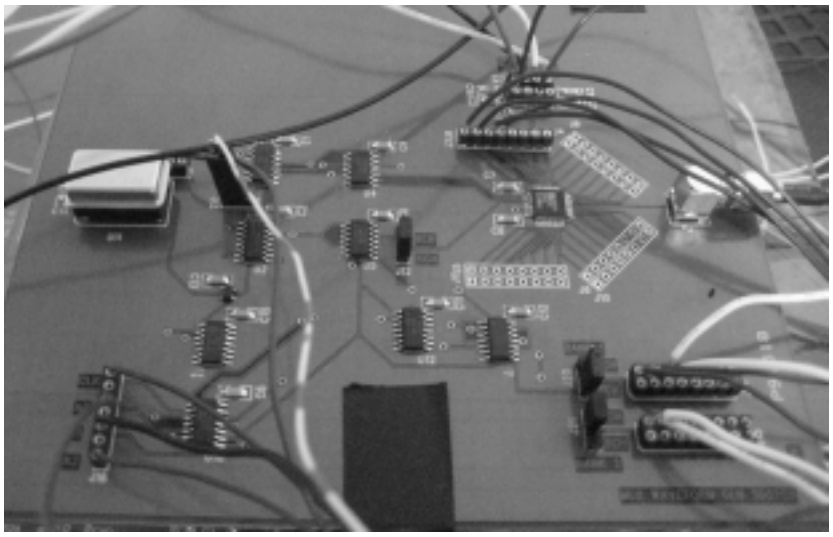

Figure 5: Multiplexer.

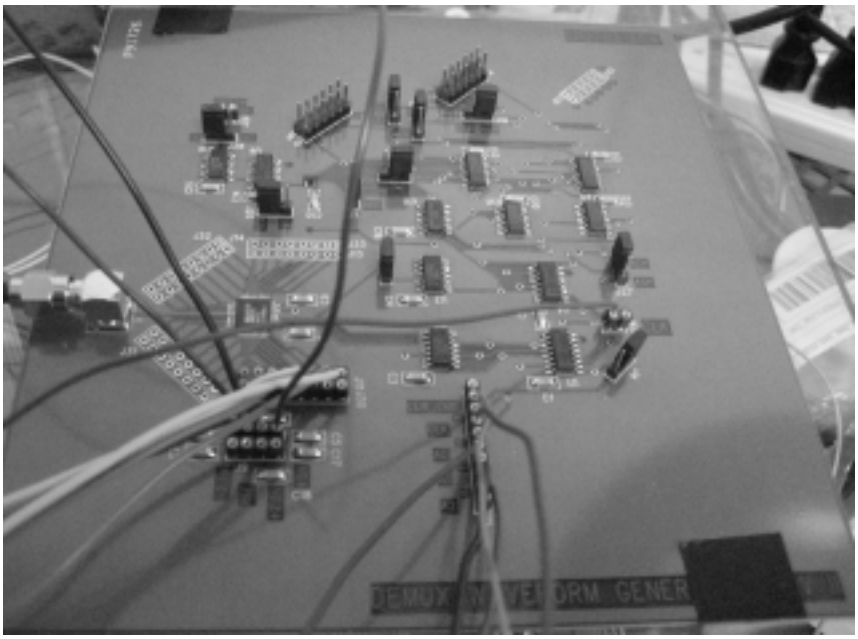

Figure 6: Demultiplexer.

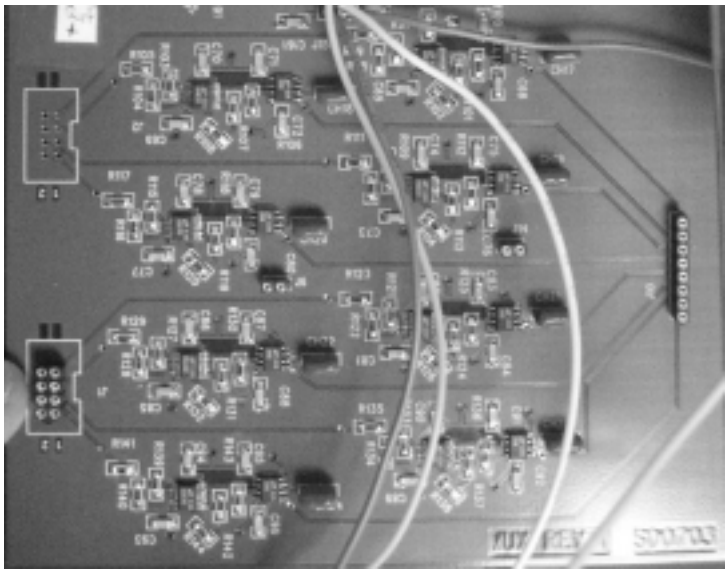

Figure 7: Multiplexer Channels 0 to 15.

10 Appendix:

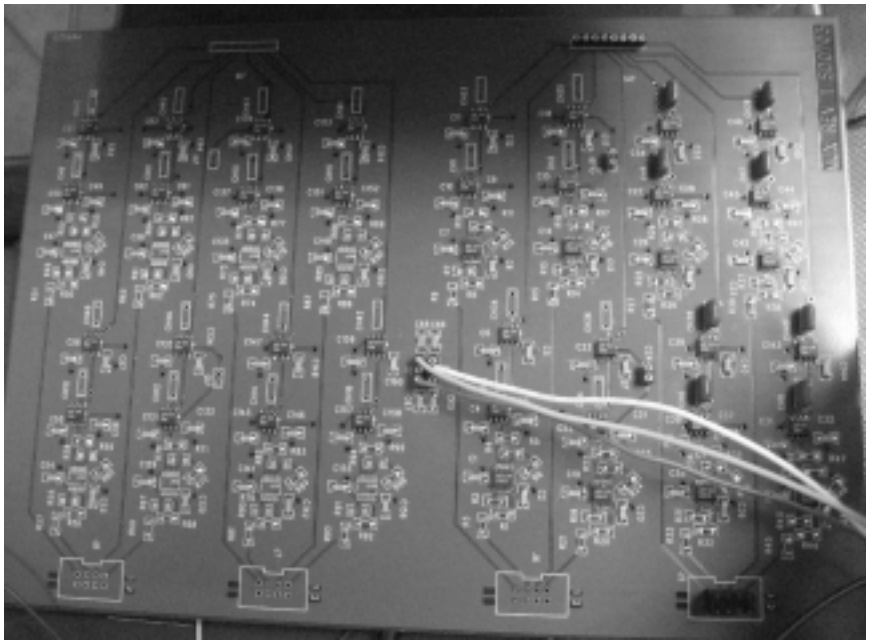

Figure 8: Multiplexer Channels 16 to 31.

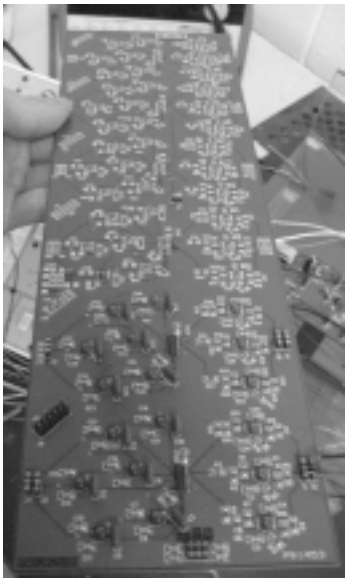

Figure 9: Demultiplexer Channels 0 to 15.

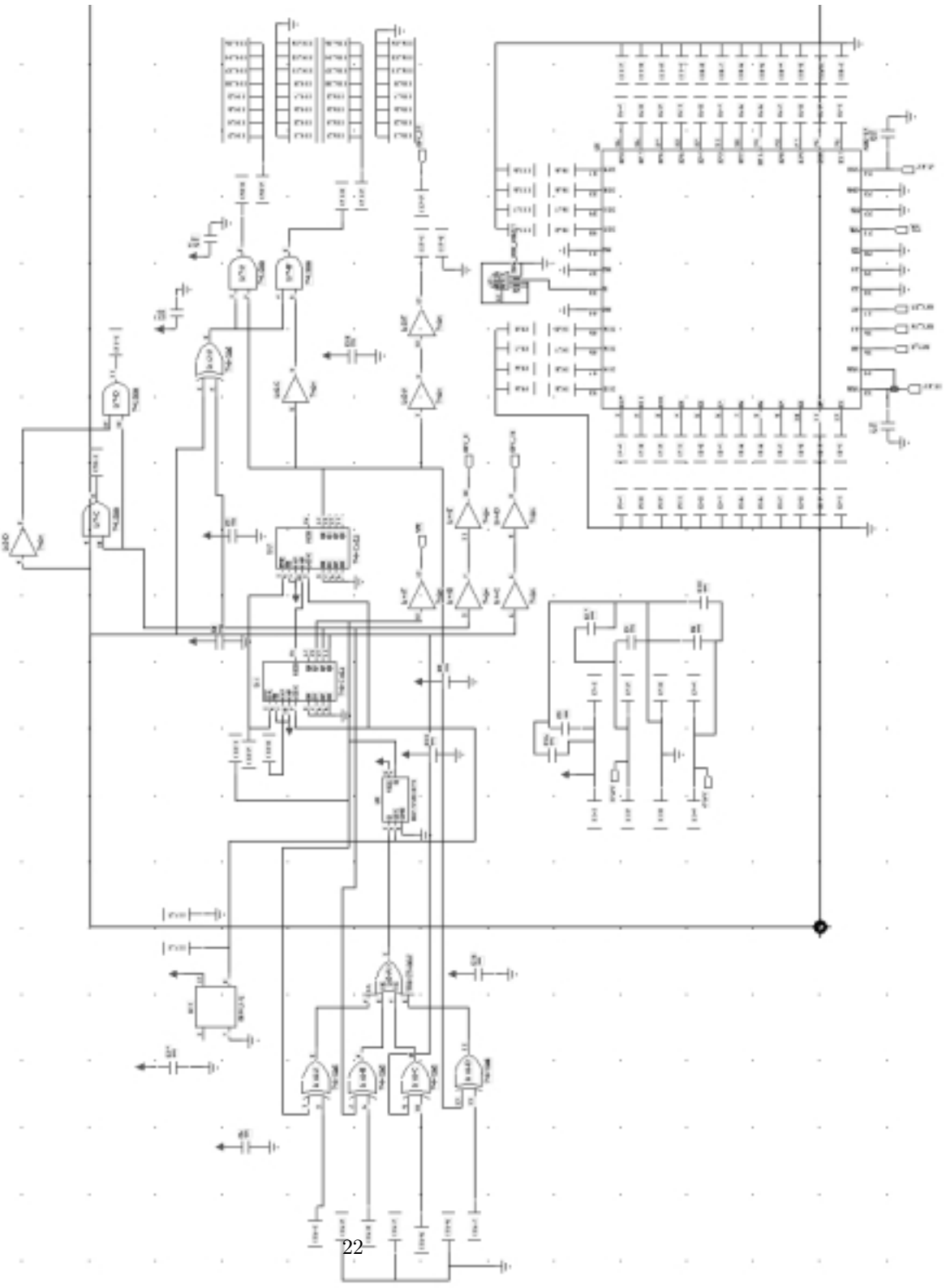

Figure 10: Multiplexer schematic

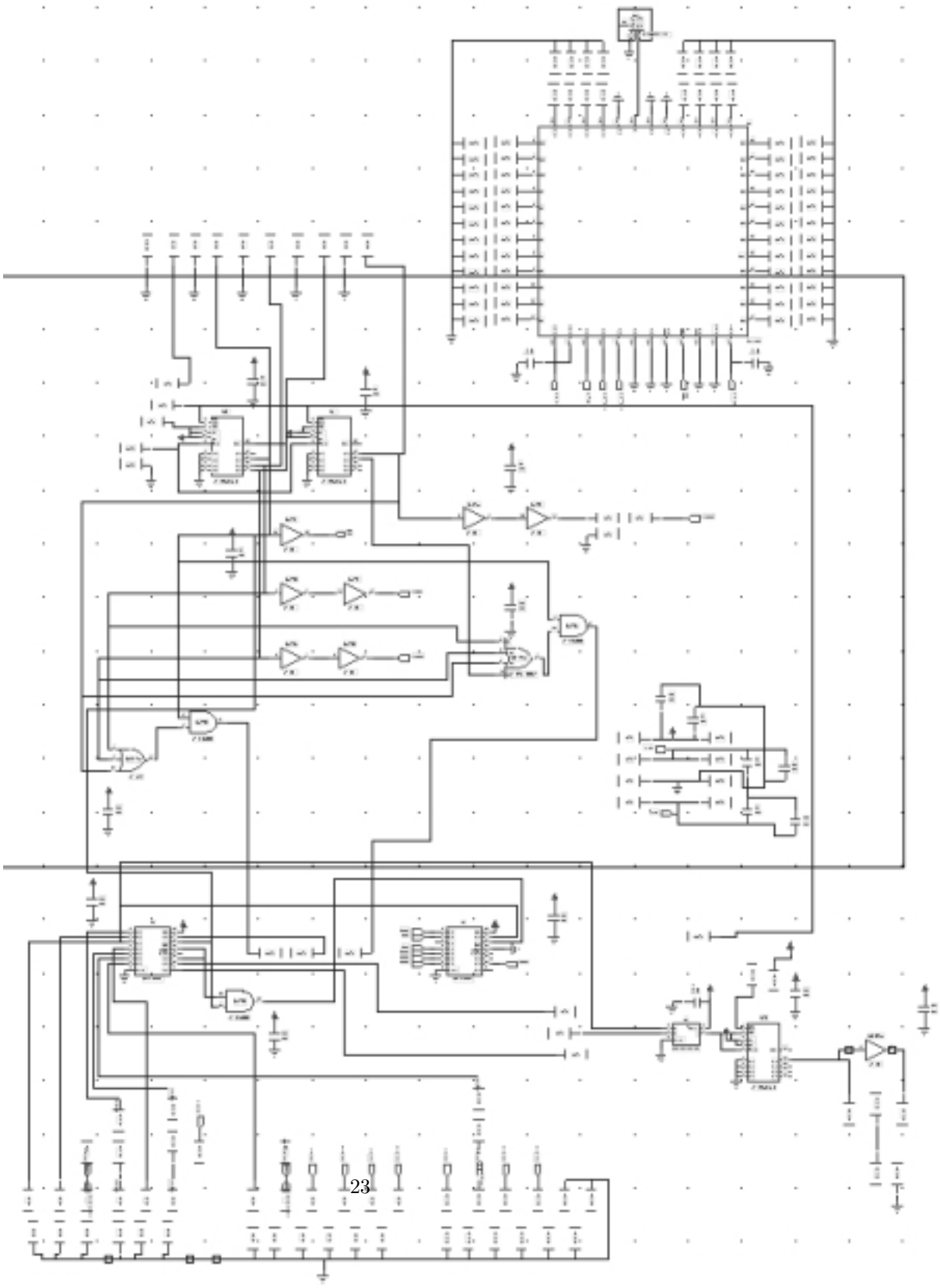

Figure 11: Demultiplexer schematic

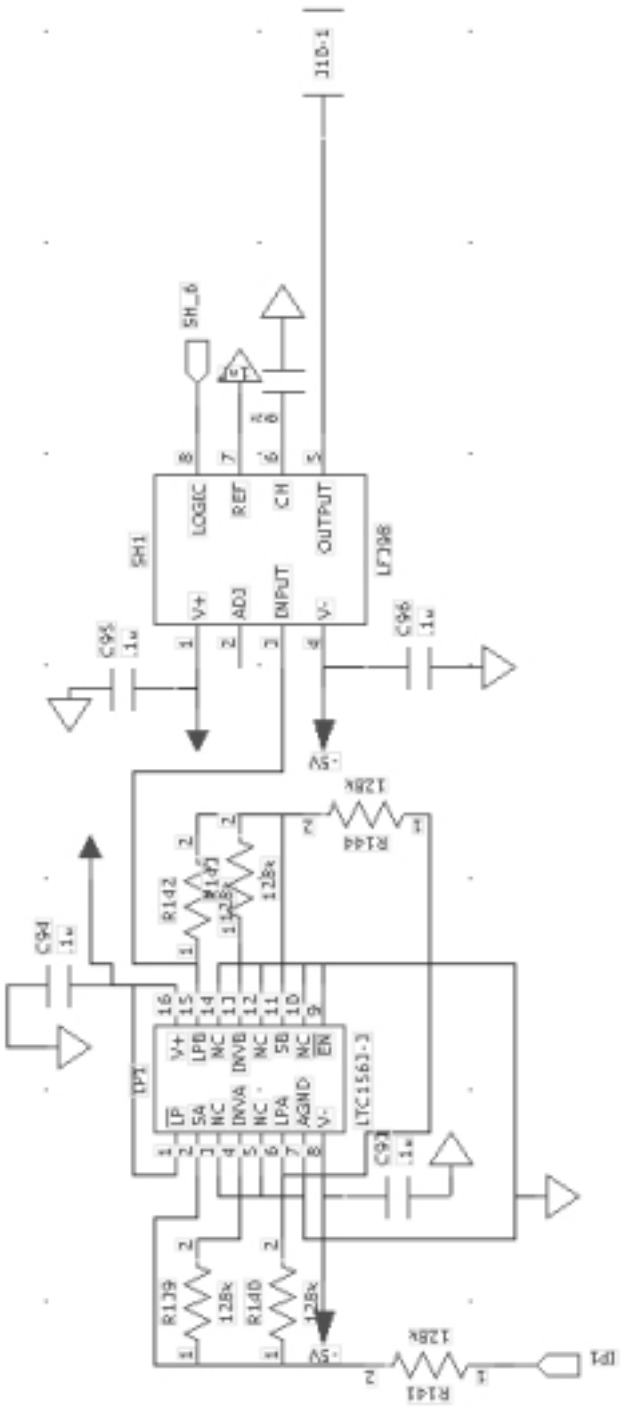

Figure 12: One channel of repeated networks on “Channels 0 to 15” schematic

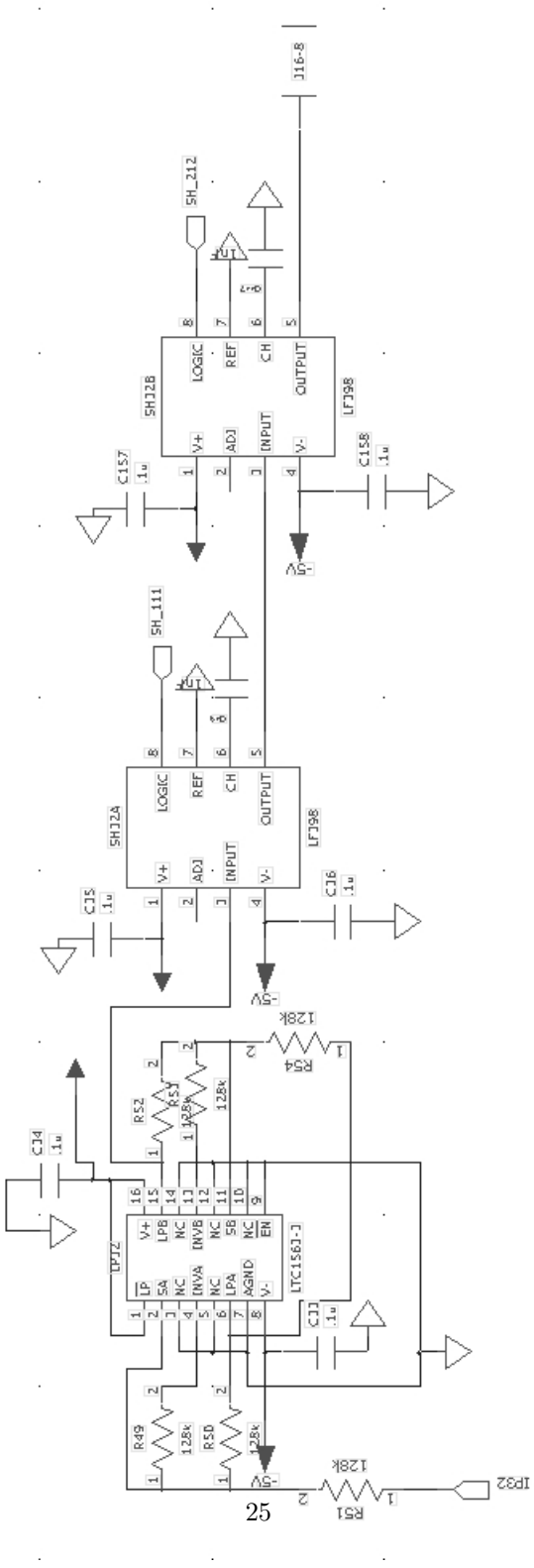

Figure 13: One channel of repeated networks on "Channels 16 to 31" schematic

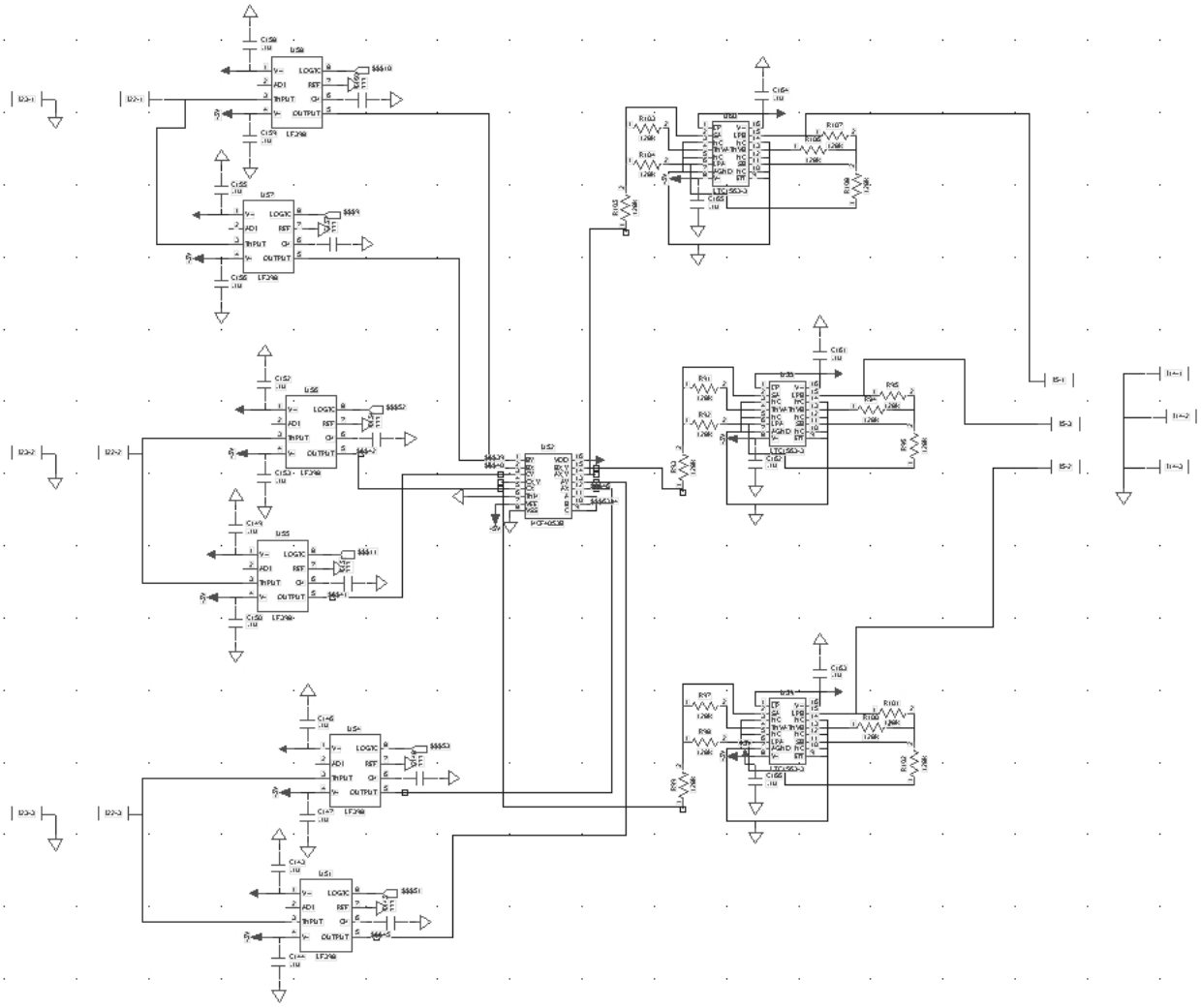

Figure 14: Three channels of repeated networks on “Demux Channels 0 to 15”

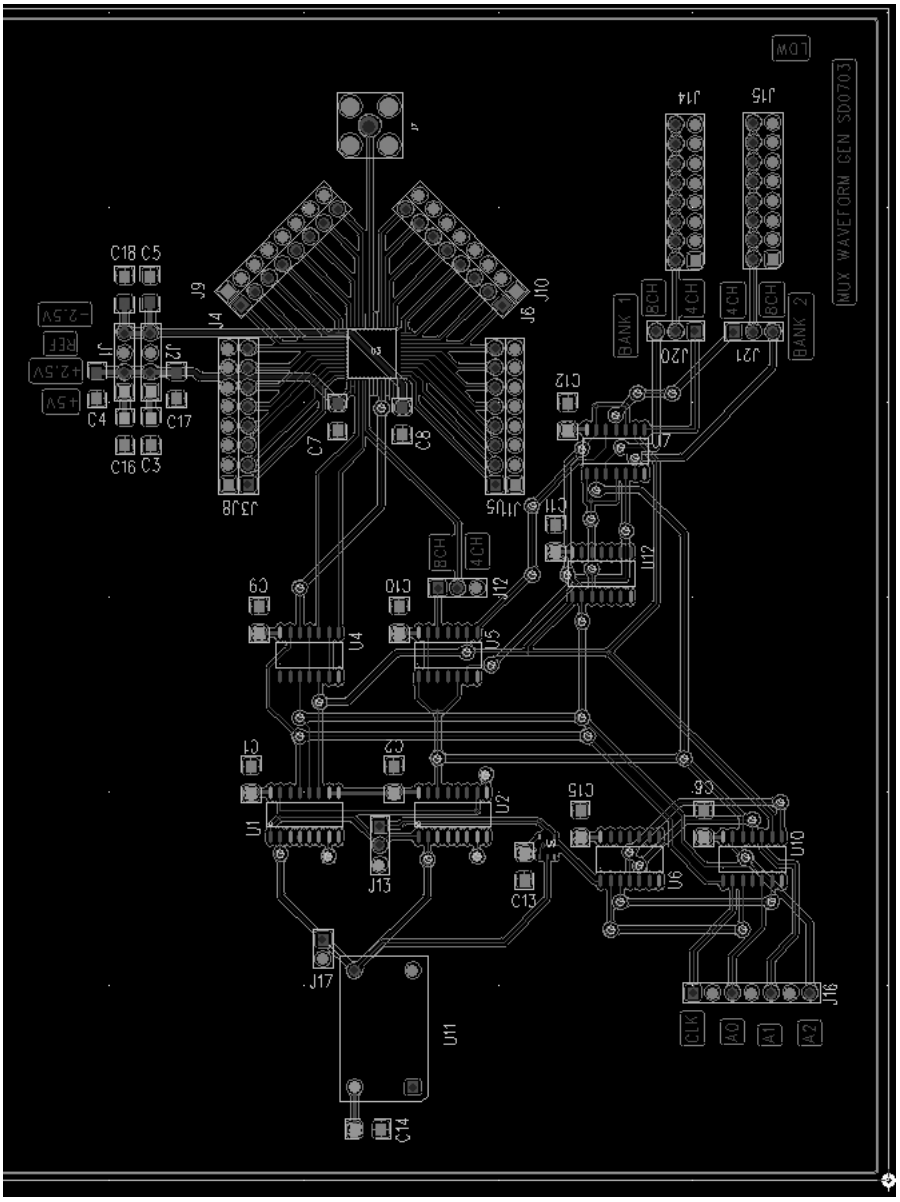

Figure 15: PADS Multiplexer layout

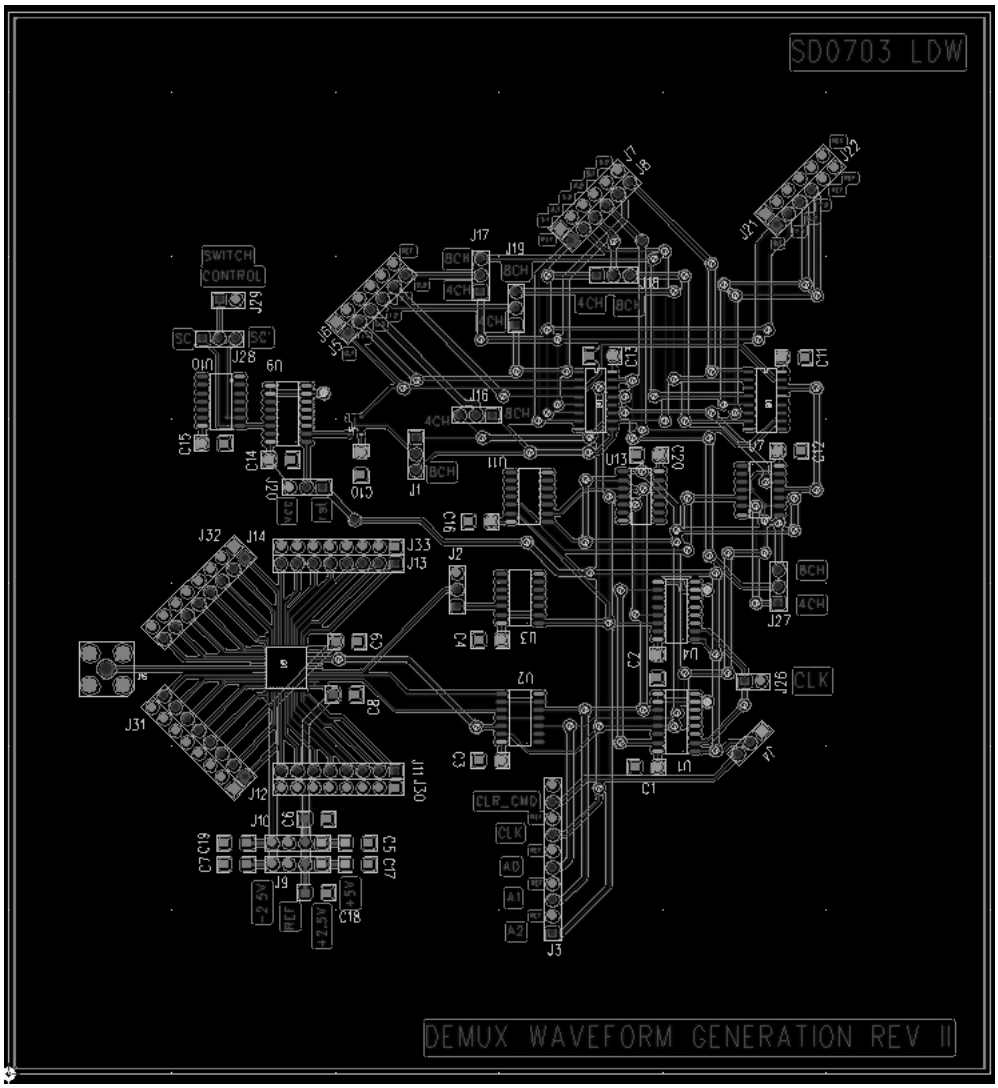

Figure 16: PADS Demultiplexer layout

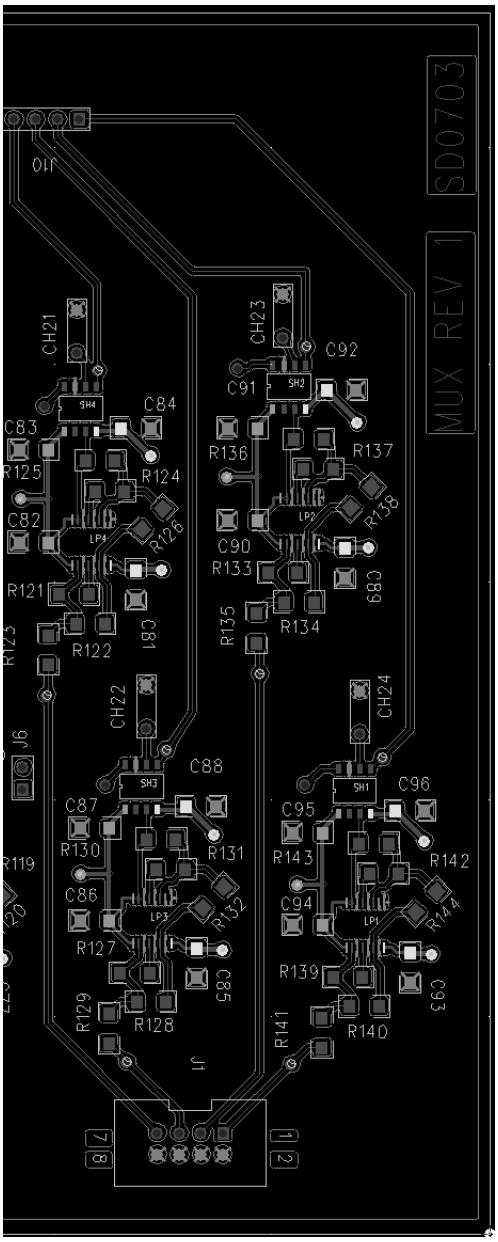

Figure 17: PADS Multiplexer layout channels 0 to 15 closeup

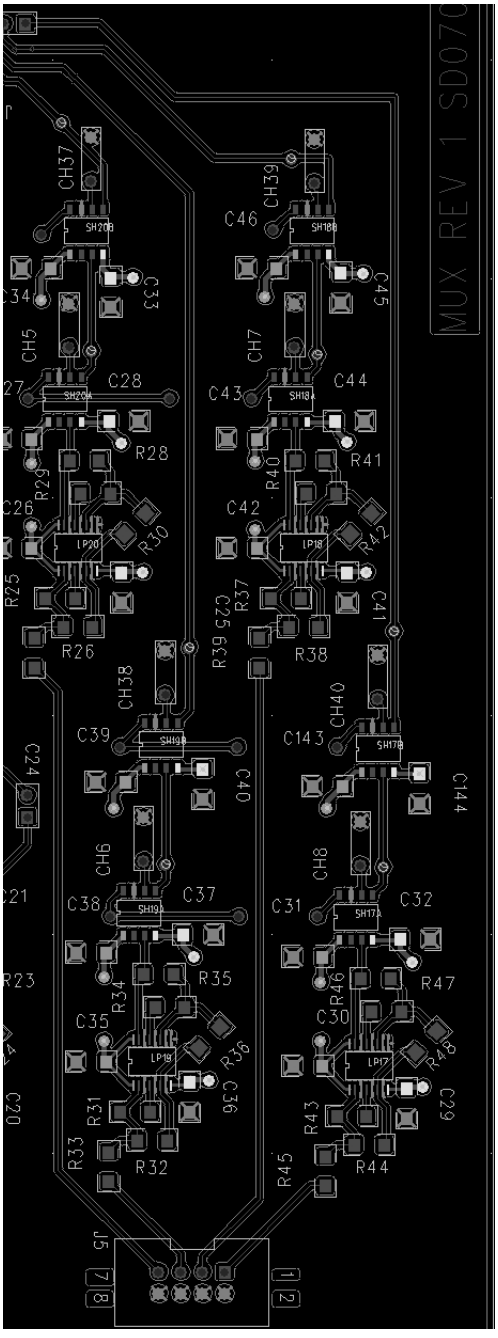

Figure 18: PADS Multiplexer layout channels 16 to 31 closeup

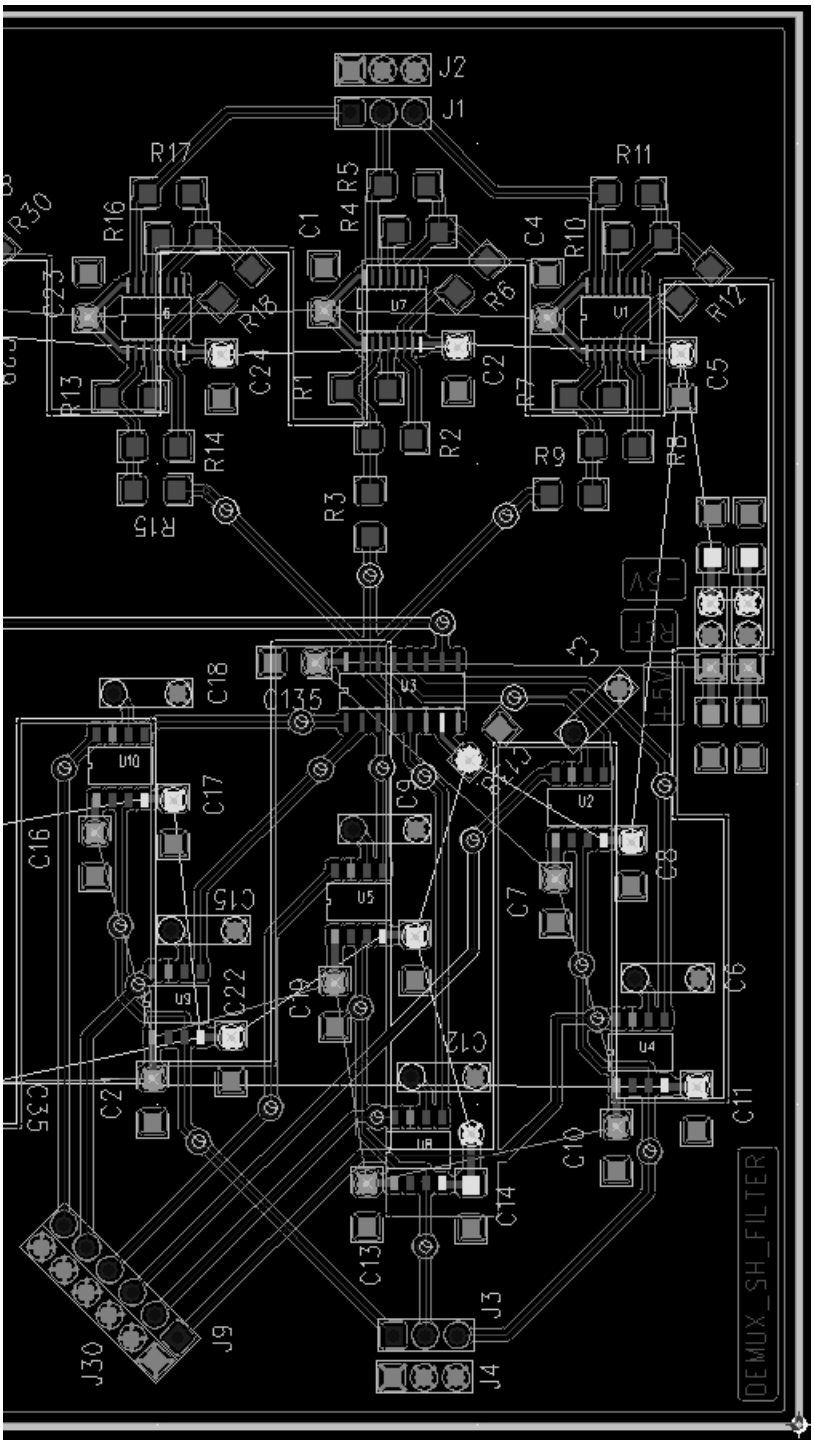

Figure 19: PADS Demultiplexer layout, all channels closeup